



AOS
SEMICONDUCTOR

产品规格说明书

Product Data Sheet

AOS8581TXF

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电源管理IC



通信接口芯片



二三极管



LDO稳压器



逻辑器件



MOSFETs



运算放大器



显示驱动



MCU单片机



光电器件



DESCRIPTIONS

The AOS8581 series of CMOS operational amplifiers use auto-zero techniques to simultaneously provide very low offset voltage (5uV max) and near-zero drift over time and temperature. This family of amplifiers has ultralow noise, offset and power.

This miniature, high-precision operational amplifiers offset high input impedance and rail-to-rail input and rail-to-rail output swing. With high gain-bandwidth product of 5MHz and slew rate of 3.4V/us.

Single or dual supplies as low as +2.7V (±1.35V) and up to +5.5V (±2.75V) may be used. The AOS8581 are specified for the extended industrial and automotive temperature range (-40°C to 125°C). The AOS8581 single amplifier is available in 5-lead SOT23 packages.

FEATURES

- Low Offset Voltage: ±1uV (TYP)
- Input Offset Drift: 0.1uV/°C
- High Gain Bandwidth Product: 5MHz
- Rail-to-Rail Input and Output
- High Gain, CMRR, PSRR: 130dB
- High Slew Rate: 3.4V/us
- Low Noise: 0.8uVp-p (0.1Hz ~ 10Hz)
- ★ Low Power Consumption: 730uA /op amp
- ★ Overload Recovery Time: 1us
- ★ Low Supply Voltage: +2.7V to +5.5V
- ★ No External Capacitors Required
- ★ Extended Temperature: -40°C to +125°C

APPLICATIONS

- Temperature Sensors
- Medical/ Industrial Instrumentation
- Pressure Sensors
- Battery-Powered Instrumentation
- Active Filtering
- Weight Scale Sensor
- Strain Gage Amplifiers
- Power Converter/ Inverter

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE(NOM)
AOS8581	SOT23-5	2.92mm × 1.62mm

(1)For all available packages, see the orderable addendum at the end of the data sheet.



PACKAGE/ORDERING INFORMATION

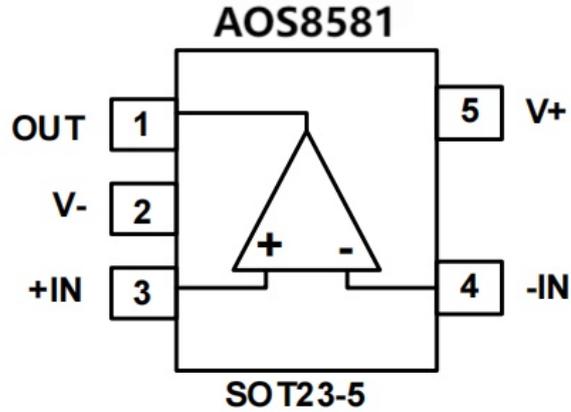
Orderable Device	Package Type	Pin	Channel	Op Temp(°C)	Device Marking ⁽¹⁾	Package Qty
AOS8581TXF	SOT23-5	5	1	-40 ~125	8581	Tape and Reel , 3000

NOTE:

- (1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.
- (2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.



PIN CONFIGURATION AND FUNCTIONS (Top View)



PIN DESCRIPTION

NAME	PIN	I/O ⁽¹⁾	DESCRIPTION
	SOT23-5		
-IN	4	I	Negative (inverting) input
+IN	3	I	Positive (noninverting) input
OUT	1	O	Output
V-	2	-	Negative (lowest) power supply
V+	5	-	Positive (highest) power supply

(1) I = Input, O = Output.



Specifications

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	Supply, $V_S=(V_+) - (V_-)$		6	V
	Signal input pin ⁽²⁾	(V ₋)-0.5	(V ₊) +0.5	
	Signal output pin ⁽³⁾	(V ₋)-0.5	(V ₊) +0.5	
Current	Signal input pin ⁽²⁾	-10	10	mA
	Signal output pin ⁽³⁾	-55	55	mA
	Output short-circuits ⁽⁴⁾	Continuous		
J_A	Package thermal impedance ⁽⁵⁾	SOT23-5	230	/W
Temperature	Operating range, T_A	-40	125	
	Junction, T_J ⁽⁶⁾	-40	150	
	Storage, T_{stg}	-65	150	

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.
- (3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.5V beyond the supply rails should be current-limited to ± 55 mA or less.
- (4) Short-circuit to ground, one amplifier per package.
- (5) The package thermal impedance is calculated in accordance with JESD-51.
- (6) The maximum power dissipation is a function of $T_{J(MAX)}$, R_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{JA}$. All numbers apply for packages soldered directly onto a PCB.



ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	± 1500	
		Machine Model (MM)	± 200	



ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V _s = (V ₊) - (V ₋)	Single-supply	2.7		5.5	V
	Dual-supply	± 1.35		± 2.75	



ELECTRICAL CHARACTERISTICS

(At $T_A = +25^\circ\text{C}$, $V_S = 4.4\text{V}$ to 36V , $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{UT} = V_S/2$, unless otherwise noted.)

PARAMETER		CONDITIONS	T_J	AOS8581			UINTS
				MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	
POWER SUPPLY							
V_S	Operating Voltage Range		25	2.7		5.5	V
I_Q	Quiescent Current /Amplifier	$V_S = \pm 2.5\text{V}$	25		730	900	μA
PSRR	Power-Supply Rejection Ratio	$V_S = 2.7\text{V}$ to 5.5V , $V_{CM} = V_S/2$	25		130		dB
			Full	100			
INPUT							
V_{OS}	Input Offset Voltage	$V_{CM} = V_S/2$	25	-5	± 1	5	μV
V_{OS} T_C	Input Offset Voltage Average Drift		Full		0.1		$\mu\text{V}/$
I_B	Input Bias Current	$V_{CM} = V_S/2$	25		± 50		pA
I_{OS}	Input Offset Current		25		± 10		pA
V_{CM}	Common-Mode Voltage Range		25	(V-) - 0.1		(V+) + 0.1	V
CMRR	Common-Mode Rejection Ratio	(V-) -0.1V < V_{CM} < (V+) +0.1V	25		130		dB
			Full	100			
OUTPUT							
A_{OL}	Open-Loop Voltage Gain	$R_L = 10\text{K}\Omega$, $V_O = 0.3\text{V}$ to 4.7V	25		130		dB
			Full	110			
V_{OH}	Output Voltage High	$R_L = 10\text{K}\Omega$ to GND	25	4.98	4.992		V
V_{OL}	Output Voltage Low	$R_L = 10\text{K}\Omega$ to V+	25		5	15	mV
I_{OUT}	Output Short-Circuit Current	$V_S = \pm 2.5\text{V}$, $V_O = 0\text{V}$	25		45		mA
C_{LOAD}	Capacitive Load Drive				100		pF



FREQUENCY RESPONSE							
SR	Slew Rate		25		3.4		V/us
GBP	Gain-Bandwidth Product		25		5		MHZ
PM	Phase Margin	$C_L=100pF$	25		60		°
tS	Setting Time, 0.1%	$V_S=\pm 2.5V,$ $C_L=100pF$	25		0.8		us
tOR	Overload Recovery Time		25		1		us
NOISE							
En	Input Voltage Noise	$f = 0.1Hz \text{ to } 10Hz,$ $V_S=\pm 2.5V$	25		0.8		μV_{PP}
en	Input Voltage Noise Density	$f = 1KHz$	25		35		nV/ Hz



TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At $T_A = +25^{\circ}\text{C}$, $V_S=5\text{V}$, $R_L=10\text{k}$ connected to $V_S/2$, $V_{OUT} = V_S/2$, unless otherwise noted.

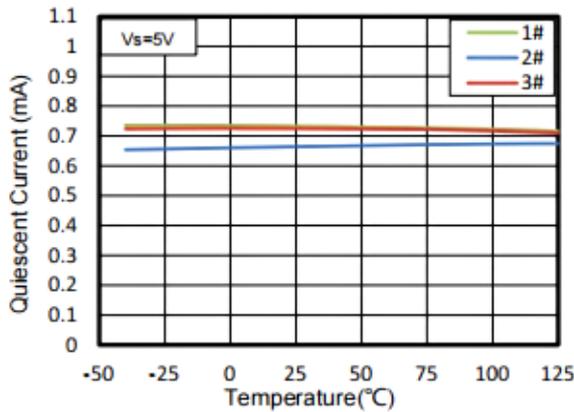


Figure 1. Quiescent Current vs Temperature

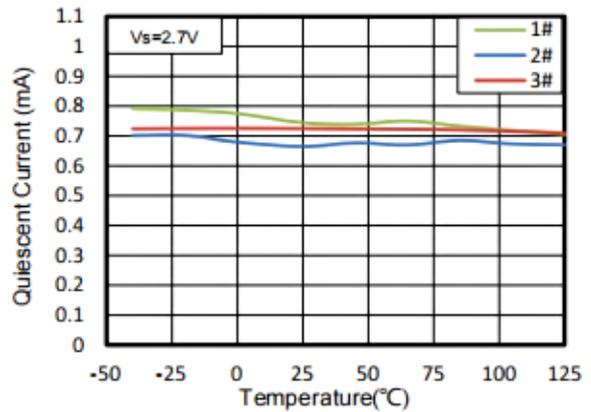


Figure 2. Quiescent Current vs Temperature

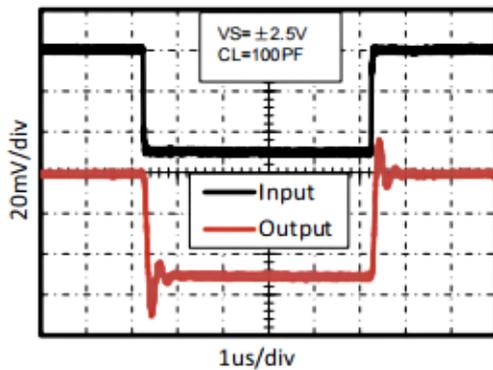


Figure 3. Small-Signal Step Response

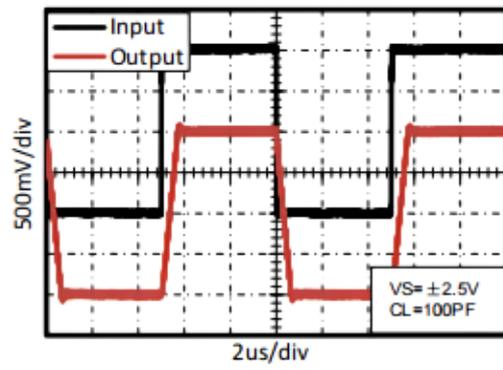


Figure 4. Large-Signal Step Response

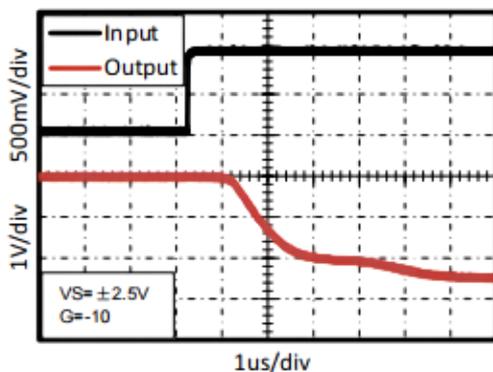


Figure 5. Positive Overvoltage Recovery

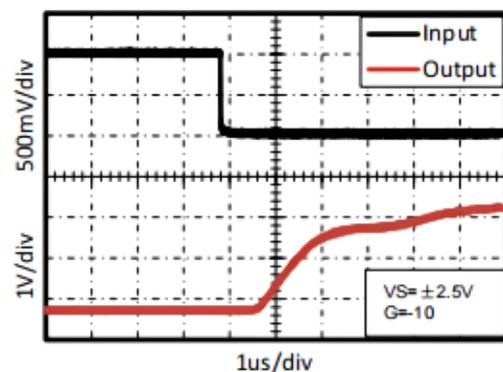


Figure 6. Negative Overvoltage Recovery

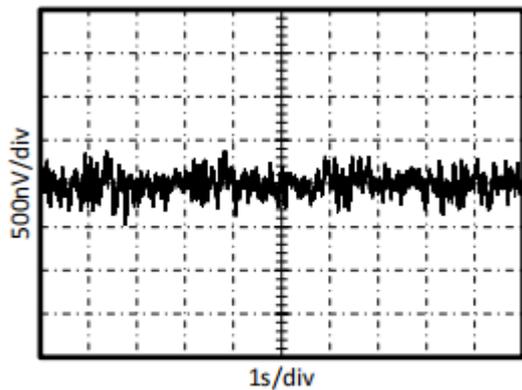


Figure 7. 0.1Hz to 10Hz Noise



Detailed Description

Overview

The AOS8581 series op amps are unity-gain stable and free from unexpected output phase reversal. They use auto-zeroing techniques to provide low offset voltage and very low drift over time and temperature.

Good layout practice mandates use of a 0.1 μ F capacitor placed closely across the supply pins.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals.

- Use low thermoelectric-coefficient connections (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat-sources.
- Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 μ V/ $^{\circ}$ C or higher, depending on materials used.

OPERATING VOLTAGE

The AOS8581 series op amps operate over a power-supply range of +2.7V to +5.5V (\pm 1.35V to \pm 2.75V). Supply voltages higher than 7V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

Application and Implementation

Information in the following applications sections is not part of the AOS component specification, and AOS does not warrant its accuracy or completeness. AOS's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

APPLICATION NOTE

The AOS8581 is a unity-gain stable, precision operational amplifier with very low offset voltage drift; these devices are also free from output phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device power-supply pins. In most cases, 0.1 μ F capacitors are adequate.

Typical Applications

Bidirectional Current-Sensing

This single-supply, low-side, bidirectional current-sensing solution detects load currents from -1A to 1A. The single-ended output spans from 110mV to 3.19V. This design uses the AOS8581 because of its low offset voltage and rail-to-rail input and output. One of the amplifiers is configured as a difference amplifier and the other provides the reference voltage.

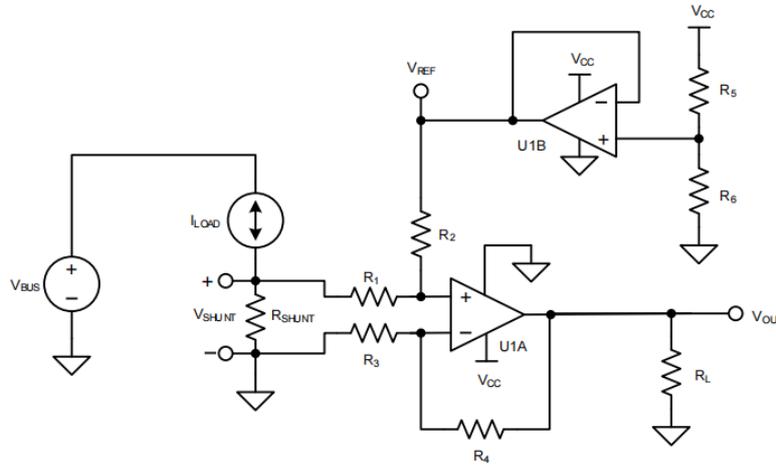


Figure 8. Bidirectional Current-Sensing Schematic

Design Requirements

This solution has the following requirements:

- Supply voltage: 3.3 V
- Input: -1 A to 1 A
- Output: 1.65 V ±1.54 V (110 mV to 3.19 V)

Detailed Design Procedure

The load current, I_{LOAD} , flows through the shunt resistor (R_{SHUNT}) to develop the shunt voltage, V_{SHUNT} . The shunt voltage is then amplified by the difference amplifier, which consists of U1A and R_1 through R_4 . The gain of the difference amplifier is set by the ratio of R_4 to R_3 . To minimize errors, set $R_2 = R_4$ and $R_1 = R_3$. The reference voltage, V_{REF} , is supplied by buffering a resistor divider using U1B. The transfer function is given by Equation 1.

$$V_{OUT} = V_{SHUNT} \times \text{Gain}_{Diff_Amp} + V_{REF}$$

Where

$$V_{SHUNT} = I_{LOAD} \times R_{SHUNT}$$

$$\text{Gain}_{Diff_Amp} = \frac{R_4}{R_3}$$

$$V_{REF} = V_{CC} \times \left[\frac{R_6}{R_5 + R_6} \right]$$

(1)



There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1 . Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4/R_3 matches R_2/R_1 . The latter value impacts the CMRR of the difference amplifier, which ultimately translates to an offset error. Because this is a low-side measurement, the value of V_{SHUNT} is the ground potential for the system load. Therefore, it is important to place a maximum value on V_{SHUNT} . In this design, the maximum value for V_{SHUNT} is set to 100 mV. Equation 2 calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100 mV and maximum load current of 1 A.

$$R_{SHUNT(Max)} = \frac{V_{SHUNT(Max)}}{I_{LOAD(Max)}} = \frac{100 \text{ mV}}{1 \text{ A}} = 100 \text{ m}\Omega \quad (2)$$

The tolerance of R_{SHUNT} is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% was selected. If greater accuracy is required, select a 0.1% resistor or better.

The load current is bidirectional; therefore, the shunt voltage range is -100 mV to 100 mV. This voltage is divided down by R_1 and R_2 before reaching the operational amplifier, U1A. Take care to ensure that the voltage present at the noninverting node of U1A is within the common-mode range of the device. Therefore, it is important to use an operational amplifier, such as the AOS8581, that has a common-mode range that extends below the negative supply voltage. Finally, to minimize offset error, note that the AOS8581 has a typical offset voltage of $\pm 1\mu\text{V}$ ($\pm 5\mu\text{V}$ maximum). Given a symmetric load current of -1 A to 1 A, the voltage divider resistors (R_5 and R_6) must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% was selected. To minimize power consumption, 10k Ω resistors were used. To set the gain of the difference amplifier, the common-mode range and output swing of the AOS8581 must be considered. Equation 3 and Equation 4 depict the typical common mode range and maximum output swing, respectively, of the AOS8581 given a 3.3V supply.

$$-100\text{mV} < V_{CM} < 3.4\text{V} \quad (3)$$

$$100\text{mV} < V_{OUT} < 3.2\text{V} \quad (4)$$

The gain of the difference amplifier can now be calculated as shown in Equation 5.

$$\text{Gain}_{\text{Diff_Amp}} = \frac{V_{OUT_Max} - V_{OUT_Min}}{R_{SHUNT} \times (I_{MAX} - I_{MIN})} = \frac{3.2 \text{ V} - 100 \text{ mV}}{100 \text{ m}\Omega \times [1 \text{ A} - (-1 \text{ A})]} = 15.5 \frac{\text{V}}{\text{V}} \quad (5)$$

The resistor value selected for R_1 and R_3 was 1k Ω . 15.4k Ω was selected for R_2 and R_4 because it is the nearest standard value. Therefore, the ideal gain of the difference amplifier is 15.4 V/V.

The gain error of the circuit primarily depends on R_1 through R_4 . As a result of this dependence, 0.1% resistors were selected. This configuration reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.



Application Curve

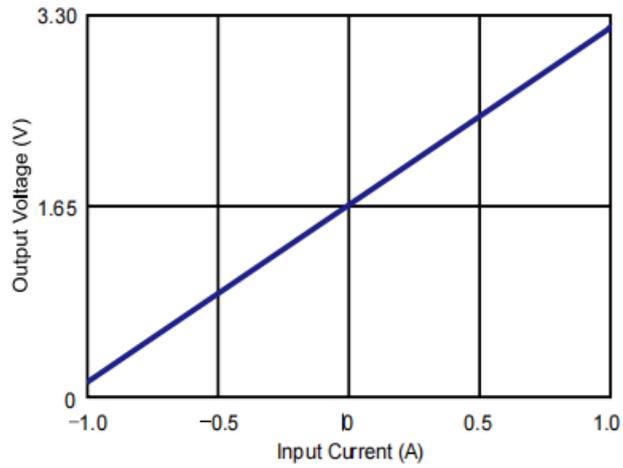
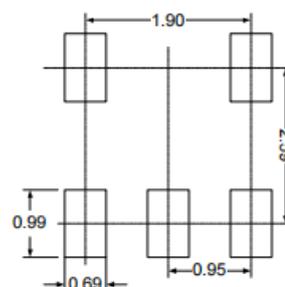
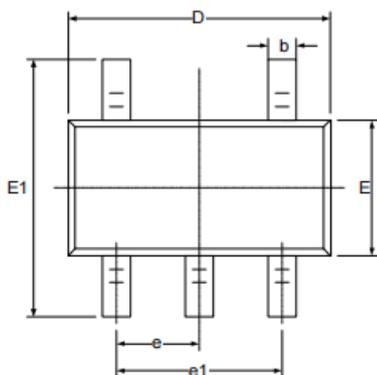


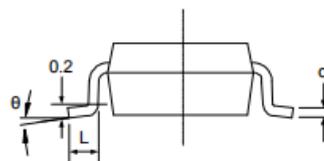
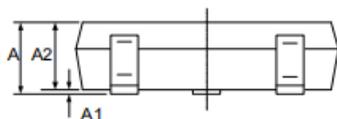
Figure 9. Bidirectional Current-Sensing Circuit Performance: Output Voltage vs Input Current



PACKAGE OUTLINE DIMENSIONS
SOT23-5



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

NOTE:

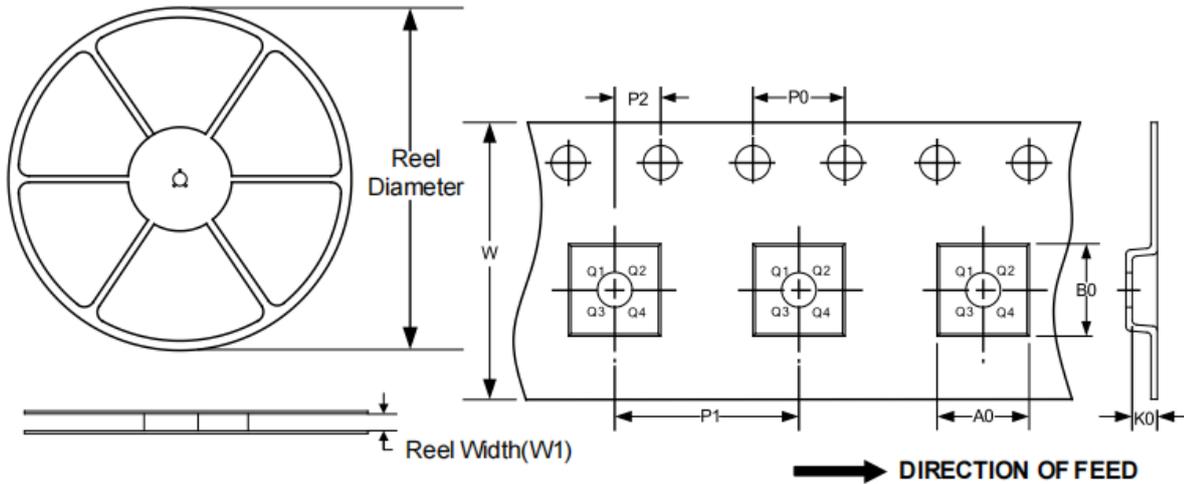
- A. All linear dimension is in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. BSC:Basic Dimension. Theoretically exact value shown without tolerances.



TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-5	7''	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3

NOTE:

1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.