



AOS
SEMICONDUCTOR

产品规格说明书

Product Data Sheet

AOS373xx

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电源管理IC



通信接口芯片



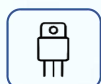
二三极管



LDO稳压器



逻辑器件



MOSFETs



运算放大器



显示驱动



MCU单片机



光电器件



Octal Transparent D-Type Latches With 3-State Outputs

DESCRIPTIONS

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The eight latches of the AOS373 devices are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

An output-enable (OE) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pull up components. OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

FEATURES

- Wide Operating Voltage Range of 1.65V to 5.5V
- High-Current 3-State True Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80 μ A Max I_{CC} \pm 6mA Output Drive at 4.5V
- Low Input Current of 1 μ A Max
- Eight High-Current Latches in a Single Package
- Full Parallel Access for Loading
- Micro Size Packages: TSSOP20, SOP20

APPLICATIONS

- Network Switches
- TV Set-top Boxes
- Motor Drives

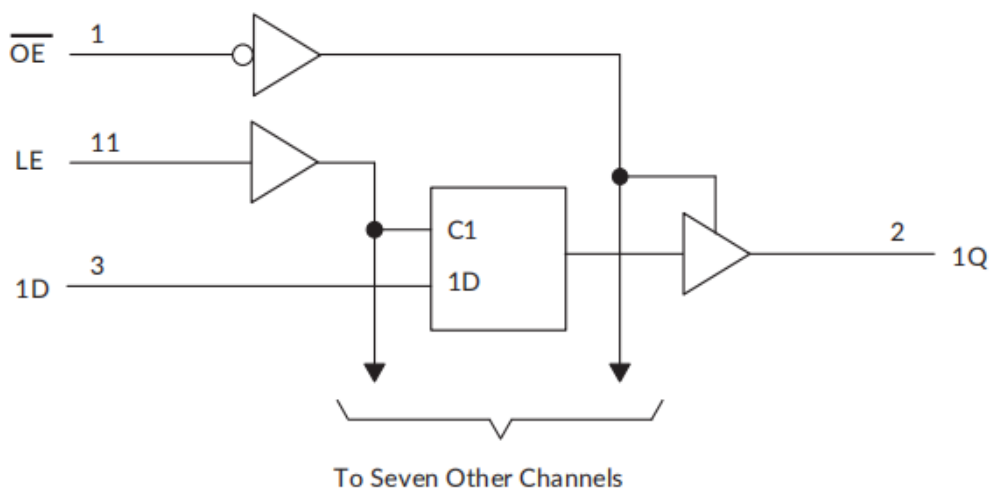
Device Information ⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AOS373	TSSOP20	6.50mm \times 4.40mm
	SOP20	12.80mm \times 7.50mm

(1)For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram



Function Table

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

NOTE:

H=High voltage level

L=Low voltage level

X=don't care

PACKAGE/ORDERING INFORMATION⁽¹⁾

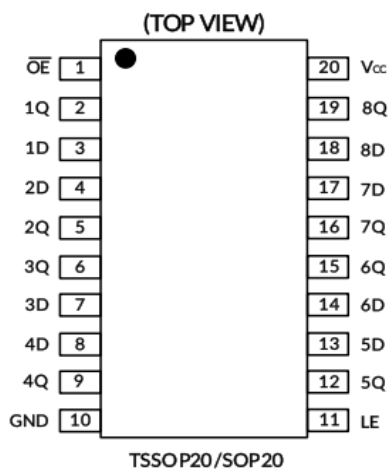
PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING ⁽²⁾	MSL ⁽³⁾	PACKAGE OPTION
AOS373	AOS373XTSS20	-40°C~+125°C	TSSOP20	AOS373	MSL3	Tape and Reel, 4000
	AOS373XS20	-40°C~+125°C	SOP20	AOS373	MSL3	Tape and Reel, 1500

NOTE:

- (1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.
- (2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.
- (3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.



PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME	I/O TYPE ⁽¹⁾	FUNCTION
TSSOP20/SOP20			
1	OE	I	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	nQ	O	3-state latch output
3, 4, 7, 8, 13, 14, 17, 18	nD	I	Data input
10	GN	P	Ground
11	OE	I	Latch enable input (active HIGH)
20	V _{cc}	P	Supply voltage

(1) I=input, O=output, P=power.



Specifications

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	6.5	V
I_{IK}	Input clamp current ⁽²⁾		± 20	mA
I_{OK}	Output clamp current ⁽²⁾		± 20	mA
I_O	Continuous output current		± 25	mA
	Continuous current through V_{CC} or GND		50	mA
J_A	Package thermal impedance ⁽³⁾	TSSOP20	40	°C/W
		SOP20	40	
T_J	Junction temperature ⁽⁴⁾	-40	150	°C
T_{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JEDEC-51.
- (4) The maximum power dissipation is a function of $T_{J(MAX)}$, R_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{JA}$. All numbers apply for packages soldered directly onto a PCB.



ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), MIL-STD-883K METHOD 3015.9	± 2000	V
		Charged-Device Model (CDM), ANSI/ESDA/JEDEC JS-002-2018	± 1000	
		Machine Model (MM), JESD22-A115C (2010)	± 200	



ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (TYP values are at $T_A = +25^{\circ}\text{C}$, Full= -40°C to 125°C , unless otherwise noted.) ⁽¹⁾



Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage	V_{CC}	Operating	1.65	5.5	V
High-level input voltage	V_{IH}	$V_{CC}=1.65V$	1.15		
		$V_{CC}=3.3V$	2.3		
		$V_{CC}=4.5V$	3.2		
		$V_{CC}=5.5V$	3.85		
Low-level input voltage	V_{IL}	$V_{CC}=1.65V$		0.5	
		$V_{CC}=3.3V$		1	
		$V_{CC}=4.5V$		1.3	
		$V_{CC}=5.5V$		1.65	
Input voltage	V_i		0	V_{CC}	
Output voltage	V_o		0	V_{CC}	
Input transition rise or fall	t/v	$V_{CC}=1.65V$		30	ns
		$V_{CC}=3.3V$		20	
		$V_{CC}=4.5V$		10	
		$V_{CC}=5.5V$		5	
Operating temperature	T_A		-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.



DC Characteristics

PARAMETER	TEST CONDITIONS	V _{CC}	TEMP	MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
V _{OH}	I _{OH} =-20μA	V _{CC} =1.65V	Full	1.55			V
		V _{CC} =3.3V		3.2			
		V _{CC} =4.5V		4.4			
		V _{CC} =5.5V		5.7			
	I _{OH} =-6.0mA	V _{CC} =4.5V		3.7			
	I _{OH} =-7.8mA	V _{CC} =5.5V		4.7			
V _{OL}	I _{OH} =-20μA	V _{CC} =1.65V	Full			0.1	
		V _{CC} =3.3V				0.1	
		V _{CC} =4.5V				0.1	
		V _{CC} =5.5V				0.1	
	I _{OH} =-6.0mA	V _{CC} =4.5V				0.4	
	I _{OH} =-7.8mA	V _{CC} =5.5V				0.4	
I _I	V _I =5.5V or GND	5.5V	25°C		±0.1	±1	μA
			Full			±2	
I _{OZ}	V _O =0V or GND, 0E=V _{IH}	5.5V	25°C			±1	
			Full			±10	
I _{CC}	V _I =5.5V or GND, I _O =0	1.65V to 5.5V	25°C			8	μA
			Full			80	
C _i		3.3V	+25°C		4	10	pF

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.
- (2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.



Timing Requirements

over recommended operating free-air temperature range($T_A=+25^{\circ}\text{C}$, unless otherwise noted)⁽¹⁾

PARAMETER			V _{CC}	V _{CC} =1.8V±0.15V			V _{CC} =2.5V±0.2V		UNIT
				MIN	TYP	MAX	MIN	MAX	
f _{dock}	Clock frequency		1.65			6		5	MHz
			3.3			18		15	
			4.5			31		25	
			5.5			33		27	
t _w	pulse width	LE HIGH	1.65	40	10		60		ns
			3.3	20	5		30		
			4.5	13	3		19.5		
			5.5	12	3		18		
t _{su}	set-up time	nD to LE	1.65	5	-8		7.5		
			3.3	5	-3		7.5		
			4.5	5	-2		7.5		
			5.5	5	-2		7.5		
t _h	hold time	nD to LE	1.65	35	10		52.5		
			3.3	15	3		22.5		
			4.5	8	2		12		
			5.5	7	2		10.5		

(1) This parameter is ensured by design and/or characterization and is not tested in production.



Switching Characteristics

over recommended operating free-air temperature range($T_A=+25^{\circ}\text{C}$, unless otherwise noted)⁽¹⁾

PARAMETER			V_{CC}	$T_A=+25^{\circ}\text{C}$			$T_A=-40^{\circ}\text{C}$		$^{\circ}\text{C}$ UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{dock}			1.65	6	12		2		MHz
			3.3	18	30		15		
			4.5	31	50		25		
			5.5	33	55		27		
t_{pd}	nD	nQ	1.65		23	34.5		39	ns
			3.3		7.5	11.5		13	
			4.5		6.5	10		11	
			5.5		6.5	10		11	
	LE	nQ	1.65		41	61.5		70	
			3.3		15	22.5		25.5	
			4.5		12.5	19		21.5	
			5.5		12.5	19		21.5	
t_{en}	OE	nQ	1.65		27.5	41.5		47	
			3.3		10.5	16		18	
			4.5		9.5	14.5		16.5	
			5.5		9	13.5		15.5	
t_{dis}	OE	nQ	1.65		21.5	32.5		37	
			3.3		11	16.5		19	
			4.5		8.5	13		14.5	
			5.5		8	12		14	
t_t		nQ	1.65		5	30		45	
			3.3		2.7	15		22	
			4.5		2.5	10		15	
			5.5		2.5	10		15	

(1) This parameter is ensured by design and/or characterization and is not tested in production.

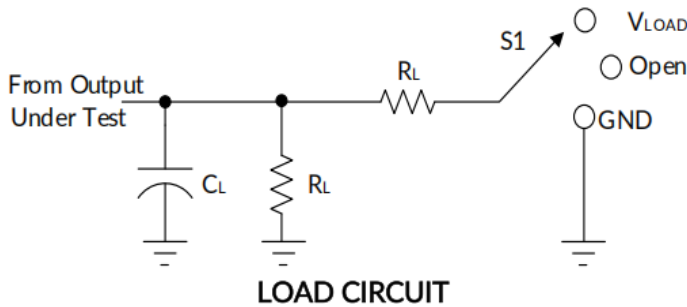
Operating Characteristics

$T_A=25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{PD}	Power dissipation capacitance per flip-flop	No load	35	pF

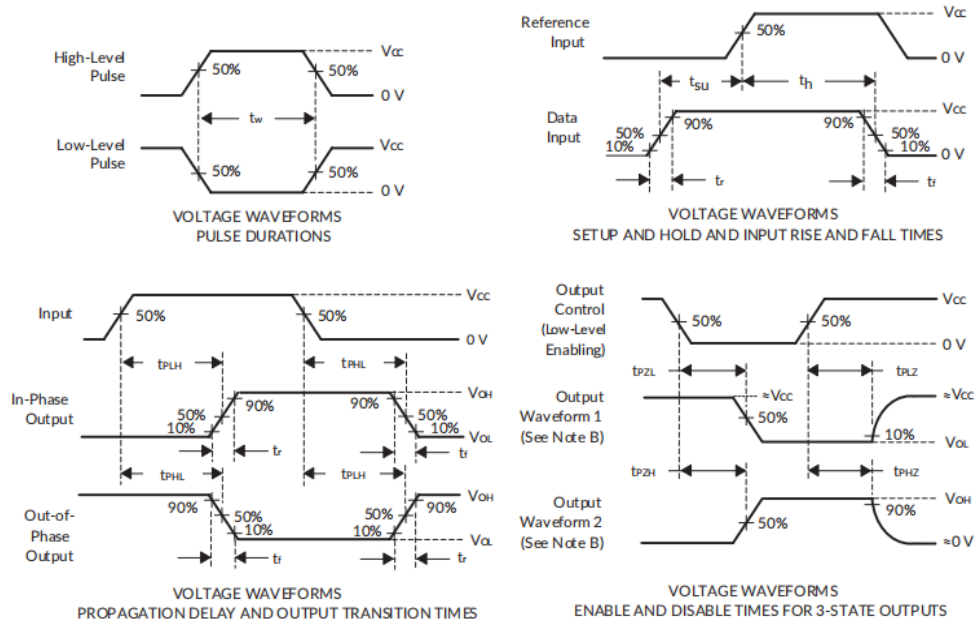


Parameter Measurement Information



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I	V_M	C_L	R_L	V_{TP}
$1.8V \pm 0.15V$	V_{CC}	$V_{CC}/2$	30pF	1k	0.15V
$2.5V \pm 0.2V$	V_{CC}	$V_{CC}/2$	30pF	500	0.15V
$3.3V \pm 0.3V$	V_{CC}	1.5V	50pF	500	0.3V
$5V \pm 0.5V$	V_{CC}	$V_{CC}/2$	50pF	500	0.3V

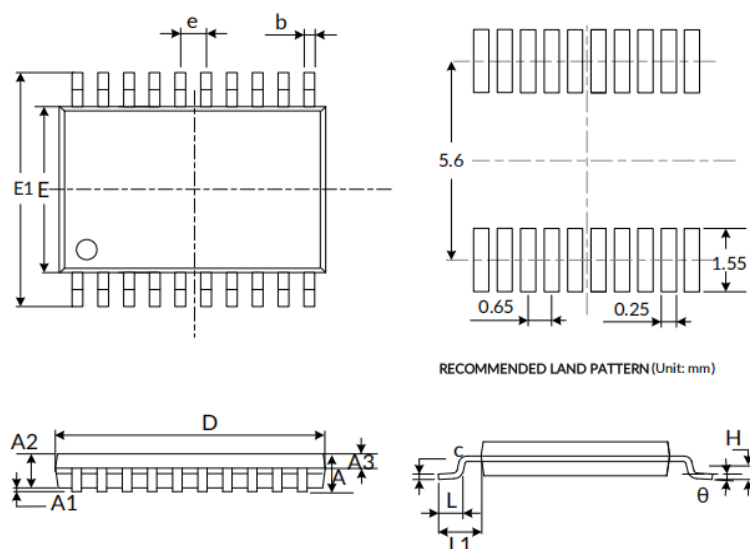


- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_0 = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



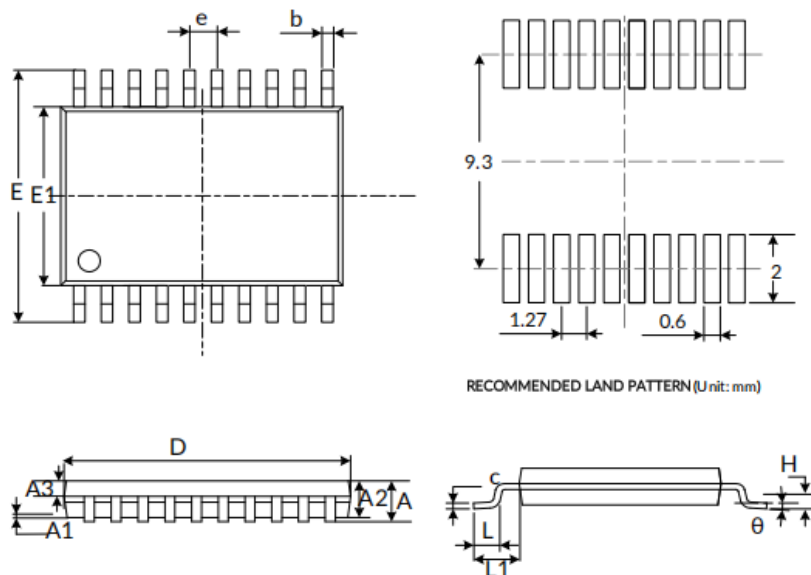
PACKAGE OUTLINE DIMENSIONS
TSSOP20⁽⁴⁾



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A ⁽¹⁾		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
A3	0.390	0.490	0.015	0.020
b	0.200	0.290	0.008	0.011
c	0.130	0.170	0.005	0.007
D ⁽¹⁾	6.400	6.600	0.252	0.260
E ⁽¹⁾	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650(BSC) ⁽²⁾		0.026(BSC) ⁽²⁾	
L	0.450	0.750	0.018	0.030
H	0.250(TYP)		0.010(TYP)	
	0°	8°	0°	8°
L1	1.00(REF) ⁽³⁾		0.039(REF) ⁽³⁾	

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. REF is the abbreviation for Reference.
4. This drawing is subject to change without notice.

SOT363(SC70-6)⁽³⁾

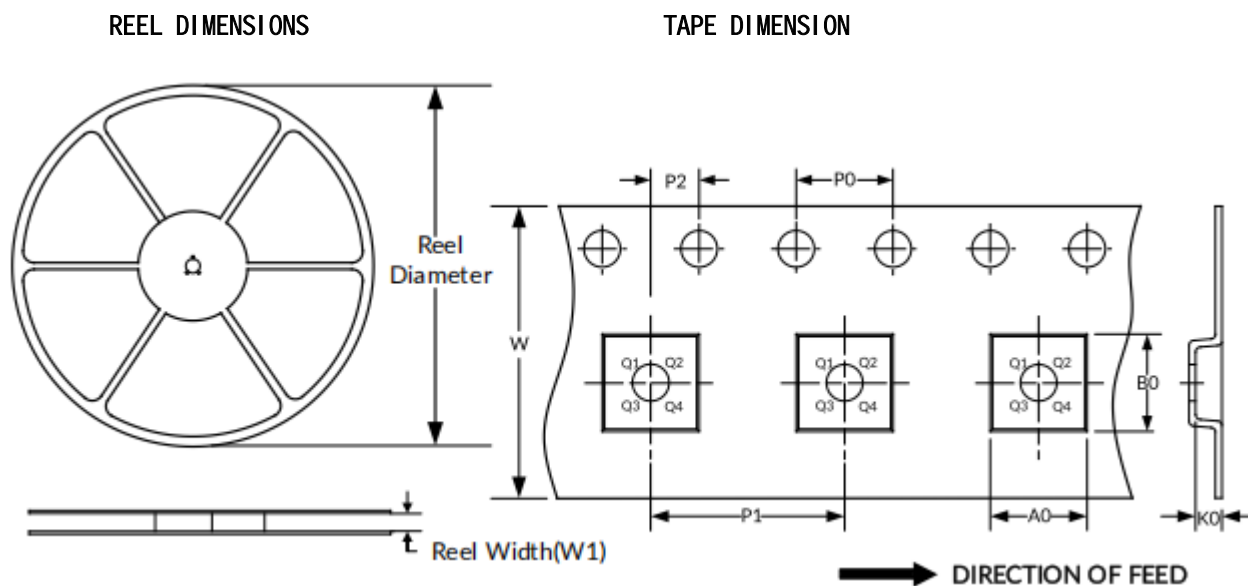
Symbol	Dimensions In Millimeters			
	Min	Max	Min	Max
A ⁽¹⁾		2.650		0.104
A1	0.100	0.300	0.004	0.012
A2	2.250	2.350	0.089	0.093
A3	0.970	1.070	0.038	0.042
b	0.390	0.470	0.015	0.019
c	0.250	0.290	0.010	0.011
D ⁽¹⁾	12.700	12.900	0.500	0.508
E ⁽¹⁾	10.100	10.500	0.398	0.413
E1 ⁽¹⁾	7.400	7.600	0.291	0.299
e	1.270(BSC) ⁽²⁾		0.050(BSC) ⁽²⁾	
L	0.700	1.000	0.028	0.039
H	0.250(TYP)		0.010(TYP)	
	0°	8°	0°	8°
L1	1.400(REF) ⁽³⁾		0.055(REF) ⁽³⁾	

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. REF is the abbreviation for Reference.
4. This drawing is subject to change without notice.



TAPE AND REEL INFORMATION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP20	13''	12.4	6.75	6.95	1.20	4.0	8.0	2.0	16.0	Q1
SOP20	13''	24.4	10.75	13.55	2.65	4.0	12.0	2.0	24.0	Q1

NOTE:

1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.