AOS SEMICONDUCTOR

产品规格说明书

Product Data Sheet

AOS2GT08xx

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AOS2GT08 Dual 2-Input Positive-AND Gate

DESCRIPTION

The AOS2GT08 dual2-input positive-AND gate is designed for 2.0 to 5.5V V_{CC} operation.The AOS2GT08 device performs the Boolean function Y=A · B or $Y=\overline{\overline{A}+\overline{B}}$ in positive logic. The device is fully + specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.The AOS2GT08 is available in Green MSOP8 and VSSOP8 packages. It operates over an ambient temperature range of -40℃ to +125℃.

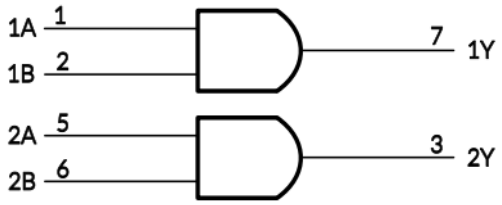
FEATURES

★ Operating Voltage Range: 2.0V to 5.5V
★ Low Power Consumption: 1μA (Max)
★ Operating Temperature Range:-40℃ to +125℃
★ Inputs Are TTL-Voltage Compatible
★ High Output Drive: ±32mA at V_{CC}=5.0V
★ MicroSize Packages: MSOP8,VSSOP8

APPLICATIONS

★ Active Noise Elimination
★ Bar Code Scanner
★ Blood Pressure Monitor
★ CPAP Machine
★ Fingerprint Identification
★ Network Attached Storage(NAS)

Simplified Schematic



Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AOS2GT08	MSOP8	3.00mm×3.00mm
	VSSOP8	2.00mm×2.30mm

(1)For all available packages, see the orderable addendum at the end of the data sheet.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	H
L	H	L
H	L	L
L	L	L

Y=A · B
H=High Voltage Level
L=Low Voltage Level

PACKAGE/ORDERING INFORMATION

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING(2)	MSL(3)	PACKAGE OPTION
AOS2GT08	AOS2GT08XM	-40℃~+125℃	MSOP8	AOS2GT08	MSL3	Tape and Reel,4000
	AOS2GT08XVS8	-40℃~+125℃	VSSOP8	2T08	MSL3	Tape and Reel,3000

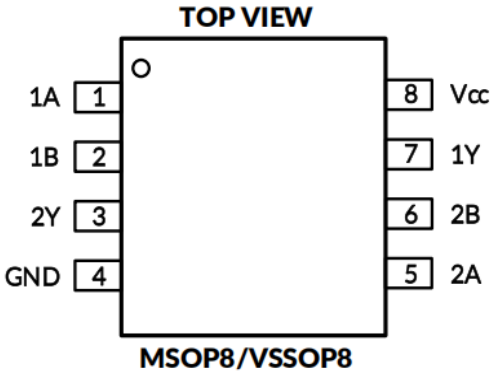
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME	I/O(1)	FUNCTION
MSOP8/VSSOP8			
1	1A	I	Channel 1 logic input
2	2B	I	Channel 1 logic input
3	2Y	O	Logic level output
4	GND	-	Ground
5	2A	I	Channel 2 logic input
6	2B	I	Channel 2 logic input
7	1Y	O	Logic level output
8	V_{CC}	-	Power Supply

(1) I=input, O=output.

Specifications

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range(2)		-0.5	6.5	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		-0.5	6.5	
V_O	Voltage range applied to any output in the high or low state(2)(3)		-0.5	V_{CC}+0.5	
I_{IK}	Input clamp current	V_I<0		-50	mA
I_{OK}	Output clamp current	V_O<0		-50	
I_O	Continuous output current			±50	
	Continuous current through V_{CC} or GND			±100	
θ_{JA}	Package thermal impedance (4)	MSOP8		170	℃/W
		VSSOP8		205	K/W
T_J	Junction temperature(5)		-65	150	℃
T_{stg}	Storage temperature		-65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

(4) The package thermal impedance is calculated in accordance with JESD-51.

(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D= ($T_{J(MAX)}$-T_A) / $R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model(HBM),per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model(CDM),per ANSI/ESDA/JEDEC JS-002(2)	±1000	
		Machine Model(MM)	±200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible todamage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (TYP values are at T_A=+25℃,Full= -40℃ to 125℃, unless otherwise noted.) (1)

Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Supply Voltage	V_{CC}	Operating	2.0	5.5	V
High-level input voltage	V_{IH}	V_{CC}=2.0V	1.0		
		V_{CC}=3.3V	1.5		
		V_{CC}=4.5V to 5.5V	2.0		
Low-level input voltage	V_{IL}	V_{CC}=2.0V		0.3	
		V_{CC}=3.3V		0.55	
		V_{CC}=4.5V to 5.5V		0.8	
Input Voltage	V_I		0	5.5	
Output Voltage	V_O		0	V_{CC}	
Input transition rise or fall	$\Delta t/\Delta v$	V_{CC}=2.0V to 5.5V		5	ns/V
Operating Temperature	T_A		-40	+125	℃

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

DC Characteristics

PARAMETER		TEST CONDITIONS	V_{CC}	TEMP	MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OH}		I_{OH}=-100μA	2.0V to 5.5V	Full	V_{CC}-0.1			V
		I_{OH}=-8mA	2.0		1.6			
		I_{OH}=-24mA	3.3		2.5			
		I_{OH}=-32mA	4.5V		3.8			
			5V		4.2			
			5.5V		4.8			
V_{OL}		I_{OH}=100μA	2.0V to 5.5V				0.1	
		I_{OH}=8mA	2.0				0.45	
		I_{OH}=24mA	3.3				0.55	
		I_{OH}=32mA	4.5V				0.55	
			5V				0.5	
			5.5V				0.45	
I_I	A or B inputs	V_I=5.5V or GND	0V to 5.5V	+25℃		±0.1	±1	μA
				Full			±5	
I_{off}		V_I or V_O=5.5V	0	+25℃		±0.1	±1	
				Full			±10	
I_{CC}		V_I=5.5V or GND, I_O=0	2.0V to 5.5V	+25℃		0.1	1	
				Full			10	
I_{CCT}		One input at 3.4V, Other inputs at V_{CC} or GND	5.5V	Full			500	
C_i(Input Capacitance)		V_{CC}=0V, f=10MHz	0V	+25℃		6		pF

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

(2) Limits are 100% production tested at 25℃. Limits over the operating temperature range are ensured through correlationsusing statistical quality control (SQC) method.

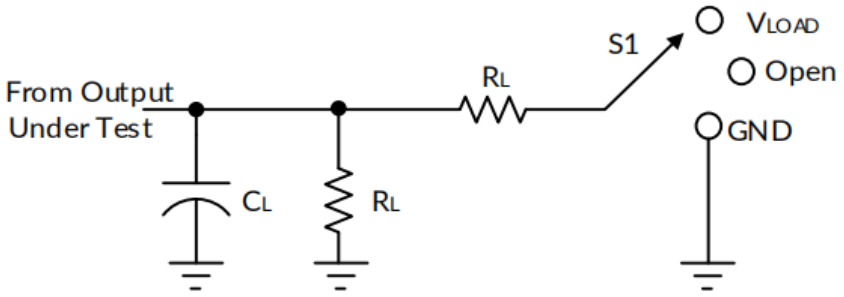
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

AC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation Delay	t_{pd}	V_{CC}=2.0V±0.2V	C_L=30pF, R_L=500Ω		15.7		ns
		V_{CC}=3.3V±0.3V	C_L=50pF, R_L=500Ω		13.8		
		V_{CC}=5V±0.5V	C_L=50pF, R_L=500Ω		4.3		
Power dissipation capacitance	C_{pd}	V_{CC}=5V	f=10MHz		22		pF

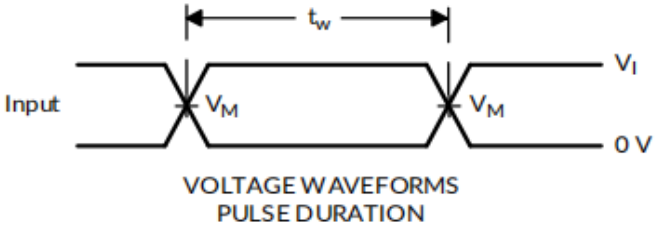
(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.
(2) This parameter is ensured by design and/or characterization and is not tested in production.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

Parameter Measurement Information

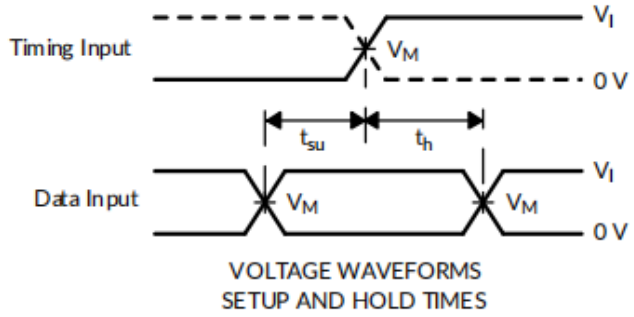


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

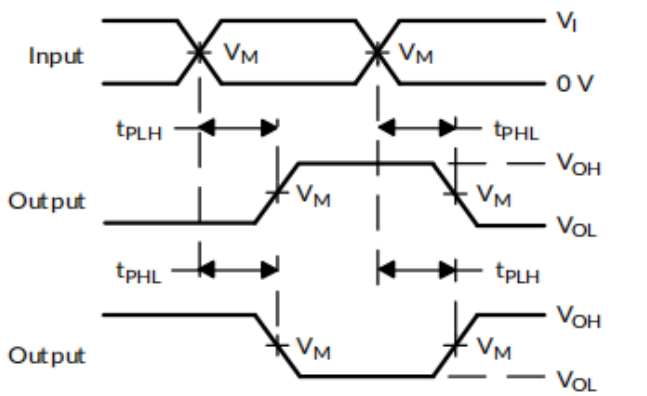
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	30pF	500Ω	0.15V
3.3V±0.3V	3V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V±0.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	2 x V_{CC}	50pF	500Ω	0.3V



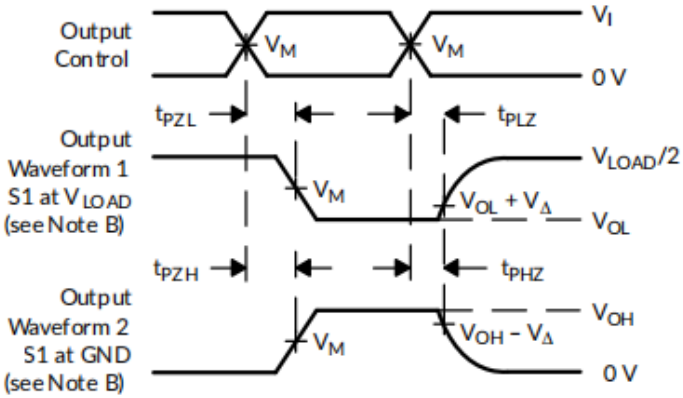
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY
TIMES INVERTION AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES
LOW-AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

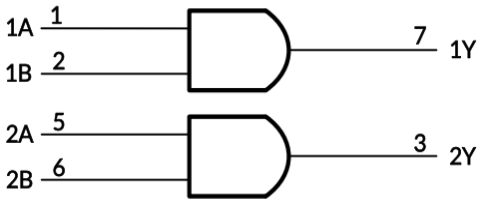
Figure 1. Load Circuit and Voltage Waveforms

Detailed Description

Overview

The AOS2GT08 deviceis a dual 2-input positive-AND gate. The device performs the Boolean AND function ($Y=A \cdot B$ or $Y=\overline{\overline{A}+\overline{B}}$) in positive logic. Low I_{CC} current allows this device to be used in power sensitive or battery powered applications. Robust inputs allow the device to up-translate with a propagation delay of 4.3ns.

Functional Block Diagram



Feature Description

- The V_{CC} for the device is optimized at 5V.
- The inputs accept V_{IH} levels of 2V.
- Output ringing is minimized by slow edge rates.
- Inputs are TTL-Voltage compatible.

Application and Implementation

Information in the following applications sections is not part of the AOS component specification, and AOS does not warrant its accuracy or completeness. AOS's customers are responsible for determining suitability of components for their purposes . Customers should validate and test their design implementation to confirm system functionality.

Application Information

The AOS2GT08 device is a single AND gate, which is often used for many common functions like power sequencing or an on LED indicator. Because the device is configured to output LOW unless all inputs are HIGH,an LED tied to the output of the device will only turn HIGH when allsystems connected are sending a HIGH, or ready signal.

Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits . The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

POWER SUPPLY RECOMMENDATIONS

The power supply pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1uF capacitor is recommended and if there are multiple VCC terminals then 0.01uF or 0.022uF capacitors are recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1μF and 1μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible.

LAYOUT

Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally, they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

Layout Example

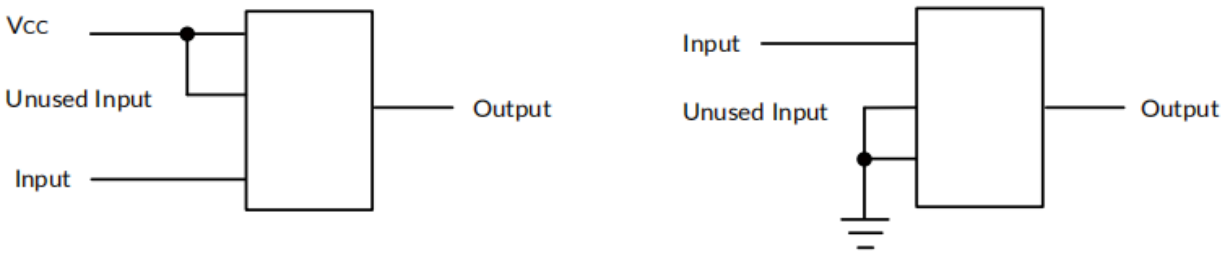
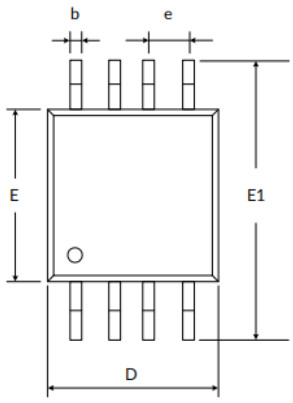
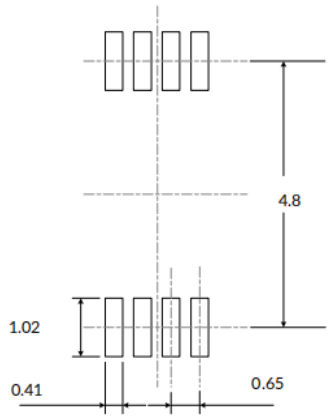


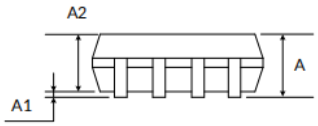
Figure 2. Layout Diagram

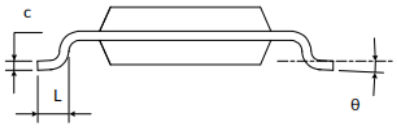
PACKAGE OUTLINE DIMENSIONS
MSOP8[3]





RECOMMENDED LAND PATTERN (Unit: mm)

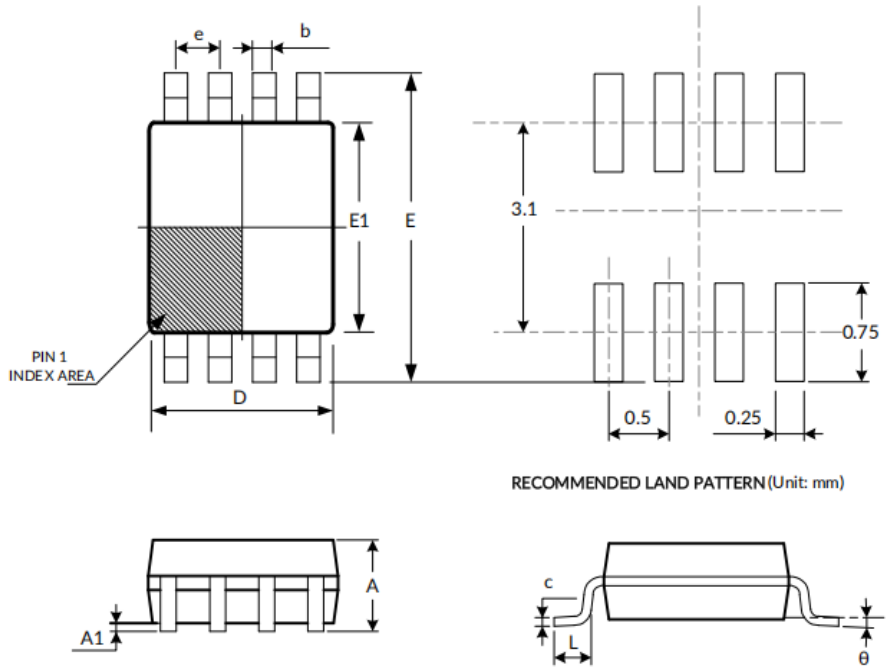




Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A[1]	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D[1]	2.900	3.100	0.114	0.122
e	0.650(BSC)[2]		0.026(BSC)[2]	
E[1]	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0 °	6 °	0 °	6 °

NOTE:
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers),"Basic" spacing is nominal.
3. This drawing is subject to change without notice.

VSSOP8[3]



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A[1]	0.600	0.900	0.024	0.085
A1	0.000	0.100	0.000	0.004
b	0.170	0.250	0.007	0.010
c	0.100	0.200	0.004	0.008
D[1]	1.900	2.100	0.075	0.083
e	0.500(BSC)[2]		0.020(BSC)[2]	
E	3.000	3.200	0.118	0.126
E1[1]	2.200	2.400	0.087	0.095
L	0.200	0.350	0.008	0.014
θ	0 °	6 °	0 °	6 °

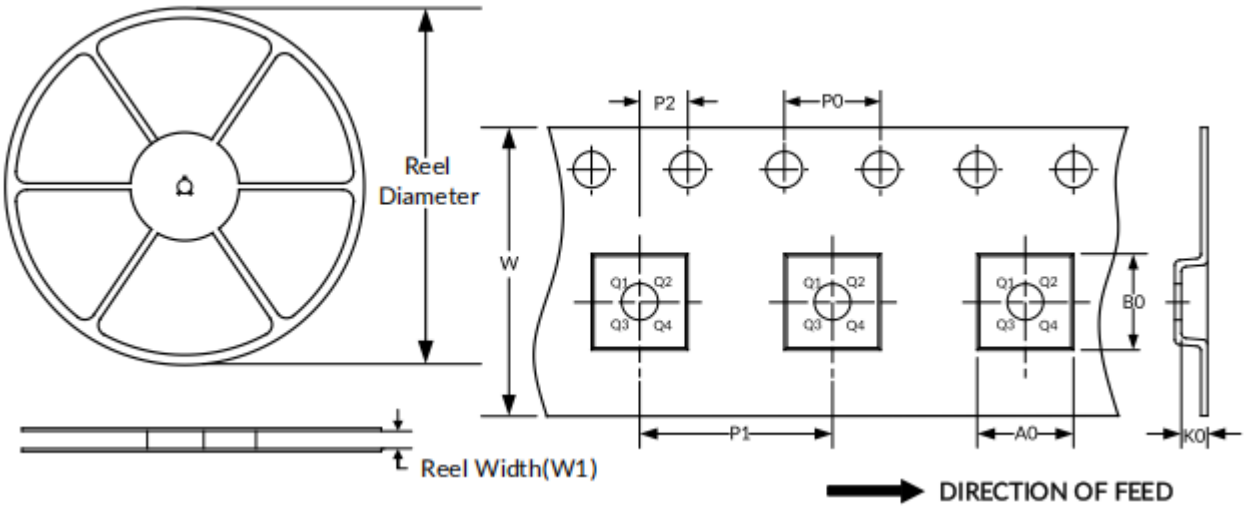
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers),"Basic" spacing is nominal.
3. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
MSOP8	13''	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1
VSSOP8	7''	9.5	2.25	3.35	1.40	4.0	4.0	2.0	8.0	Q3

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.