



AOS
SEMICONDUCTOR

产品规格说明书

Product Data Sheet

AOS244Txx

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电源管理IC



通信接口芯片



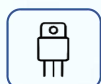
二三极管



LDO稳压器



逻辑器件



MOSFETs



运算放大器



显示驱动



MCU单片机



光电器件



Octal Buffer/Driver With 3-State Outputs

DESCRIPTIONS

The AOS244T is organized as two 4-bit buffers or drivers with separate output enable (\overline{OE}) inputs. The 3-state outputs are controlled by the output enable inputs 1 \overline{OE} and 2 \overline{OE} . A HIGH on \overline{OE} causes the outputs are in the high-impedance state. While A Low on \overline{OE} , the devices passes data from input A to output Y. Supply voltage operates from 4.5V to 5.5V.

FEATURES

Power-Supply Range: 4.5V to 5.5V
3-State Outputs Drive Bus Lines
Low Power Consumption: $40\mu A$ $I_{CC}(\text{Max})$
TTL Input are Compatible
 $\pm 24mA$ Output Drive at 5V
 V_{CC} Isolation: If V_{CC} is at GND, Both Ports are in the High-Impedance State
 I_{OFF} : Supports Partial-Power-Down Mode Operation
Extended Temperature: $-40^{\circ}C$ to $125^{\circ}C$
Micro Size Packages: TSSOP20, SOP20

APPLICATIONS

Servers
LED Displays
Network Switches
Smart Grids
Power Infrastructure
Motor Drivers
I/O Expanders
Tests and Measurements

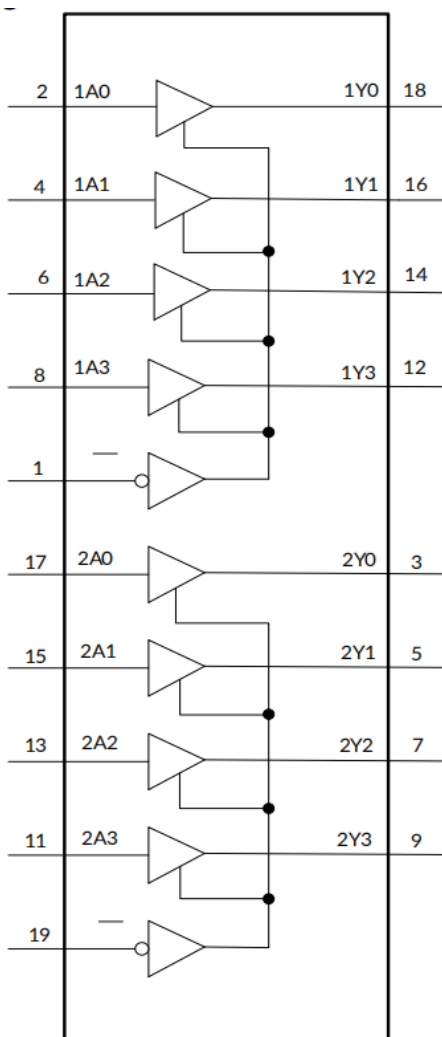
Device Information ⁽¹⁾

PARTNUMBER	PACKAGE	BODY SIZE(NOM)
AOS244T	TSSOP20	6.50mm × 4.40mm
	SOP20	12.80mm × 7.50mm

(1)For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram



Function Table

INPUTS		OUTPUT
\overline{OE}	A PORT	Y PORT
L	H	H
L	L	L
H	X	Hi-Z

NOTE:

H=HIGH voltage level

L=LOW voltage level

X=Don't care

Z=High impedance OFF-state



PACKAGE/ORDERING INFORMATION⁽¹⁾

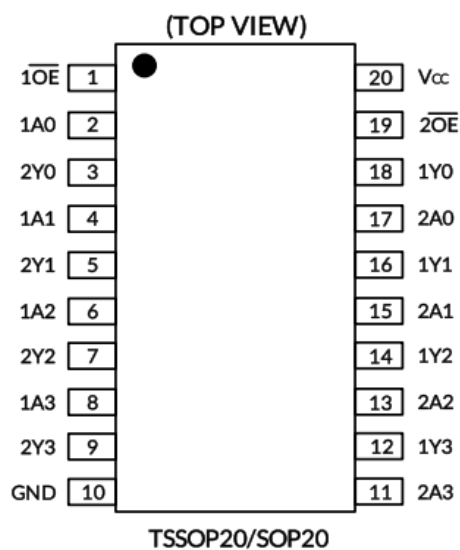
PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING ⁽²⁾	MSL ⁽³⁾	PACKAGE OPTION
AOS244T	AOS244TXTSS20	-40 ~+125	TSSOP20	AOS244T	MSL3	Tape and Reel, 4000
	AOS244TXS20	-40 ~+125	SOP20	AOS244T	MSL3	Tape and Reel, 1500

NOTE:

- (1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.
- (2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.
- (3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.



PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME	TYPE ⁽¹⁾	FUNCTION
TSSOP20/SOP20			
1	1 \overline{OE}	I	Output Enable (Active Low). Pull 1 \overline{OE} high to place all outputs in 3-state mode.
2	1A0	I	Input
3	2Y0	O	Output
4	1A1	I	Input
5	2Y1	O	Output
6	1A2	I	Input
7	2Y2	O	Output
8	1A3	I	Input
9	2Y3	O	Output
10	GND	G	Ground.
11	2A3	I	Input
12	1Y2	O	Output
13	2A2	I	Input
14	1Y2	O	Output
15	2A1	I	Input
16	1Y1	O	Output
17	2A0	I	Input
18	1Y0	O	Output
19	2 \overline{OE}	I	Output Enable (Active Low). Pull 2 \overline{OE} high to place all outputs in 3-state mode.
20	V _{cc}	P	Supply voltage. 4.5V ≤ V _{cc} ≤ 5.5V

(1) I=input, O=output, P=power, G=Ground.



SPECIFICATIONS

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

SYMBOL	PARAMETER		MIN	MAX	UNIT
V_{CC}	Supply Voltage Range		-0.5	6.5	V
V_I ⁽²⁾	Input Voltage Range		-0.5	$V_{CC}+0.5$	
V_O ⁽²⁾⁽³⁾	Output Voltage Range		-0.5	$V_{CC}+0.5$	
I_{IK}	Input Clamp Current	$V_I < 0$		± 20	mA
I_{OK}	Output Clamp Current	$V_O < 0$		± 20	
I_O	Continuous output current			± 50	
	Continuous current through V_{CC} or GND			± 200	
J_A	Package thermal impedance ⁽⁴⁾	TSSOP20		40	°C/W
		SOP20		40	
T_J	Junction Temperature ⁽⁵⁾		-40	150	°C
T_{stg}	Storage Temperature		-65	150	

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} are provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD-51.
- (5) The maximum power dissipation is a function of $T_{J(MAX)}$, R_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{JA}$. All numbers apply for packages soldered directly onto a PCB.



ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2000	V
		Charged-Device Model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	± 1000	
		Machine Model (MM)	± 200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.



ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



Recommended Operating Conditions

V_{CC} is the supply voltage associated with the input port and output port. ⁽¹⁾⁽²⁾

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		4.5		5.5	V
High-Level Input Voltage	V_{IH}	$V_{CC}=4.5V$ to $5.5V$	2			
Low-Level Input Voltage	V_{IL}	$V_{CC}=4.5V$ to $5.5V$			0.8	
Input Voltage	V_I		0		V_{CC}	
Output Voltage	V_O		0		V_{CC}	
High-Level Output Current	I_{OH}	$V_{CC}=4.5V$ to $5.5V$			-24	mA
Low-Level Output Current	I_{OL}	$V_{CC}=4.5V$ to $5.5V$			24	
Input transition rise or fall rate	$\Delta t / \Delta v$	$V_{CC}=4.5V$ to $5.5V$			8	ns/V
Operating free-air Temperature	T_A		-40		125	°C

- (1) All unused or driven (floating) data inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably V_{CC} or GND) to ensure proper device operation and minimize power.
- (2) All unused control inputs must be held at V_{CC} or GND to ensure proper device operation and minimize power consumption.

**ELECTERICAL CHARACTERISTICS**

over recommended operating free-air temperature range (TYP values are at TA =+25°C, Full =-40°C to 125°C, unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	TEMP	MIN ⁽¹⁾	TYP ⁽²⁾	MAX ⁽¹⁾	UNIT
V _{OH}	I _{OH} = -50μA	4.5V	FULL	4.4			V
		5.5V		5.4			
	I _{OH} = -24mA	4.5V		3.76			
		5.5V		4.76			
	I _{OH} = -50mA	5.5V		3.85			
V _{OL}	I _{OH} = 50μA	4.5V	FULL			0.1	
		5.5V				0.1	
	I _{OH} = 24mA	4.5V				0.73	
		5.5V				0.69	
	I _{OH} = 50mA	5.5V				1.65	
I _I	V _I =V _{CC} or GND	5.5V	+25°C			± 1	
			FULL			± 2	
I _{off}	V _I or V _O =0 to 5.5V	0V	+25°C			± 1	μA
			FULL			± 2	
I _{OZ} ⁽³⁾	V _O =V _{CC} or GND; V _I =V _{IH} or V _{IL}	5.5V	+25°C			± 1	
			FULL			± 2.5	
I _{CC}	V _I =V _{CC} or GND ⁽⁴⁾ ; I _O =0	5.5V	+25°C			4	
			FULL			40	
I _{CC}	One input at 3.4V, Other inputs at GND or V _{CC}	5.5V	+25°C		0.6		mA
			FULL			1.5	
C _I	V _I =V _{CC} or GND	5V	+25°C		3.3		pF
C _O	V _O =V _{CC} or GND	5V	+25°C		5.5		

- (1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
- (2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
- (3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
- (4) Hold all unused data inputs of the device at V_{CC} or GND to assure proper device operation.



Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 5V \pm 0.5V$ (unless otherwise noted).

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}^{(1)}$			$T_A = -40 \sim 125^\circ\text{C}^{(1)}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	An	Yn	2.5	5.1	8.1	2.4		9.3	ns
t_{PHL}			2.4	5.0	8.0	2.3		9.0	
t_{PHZ}	\overline{OE}	Yn	2.1	4.6	7.8	2.0		8.4	
t_{PLZ}			2.6	5.4	8.4	2.4		9.9	
t_{PZH}	\overline{OE}	Yn	3.0	6.4	12.0	2.0		13.0	
t_{PZL}			1.4	3.3	5.7	1.0		9.5	

(1) This parameter is ensured by design and/or characterization and is not tested in production.



Operating Characteristics

$T_A=25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC}=5\text{V}$	UNIT
			TYP	
$C_{pd}^{(1)}$	Power dissipation capacitance per buffer/driver	$C_L=50\text{pF}$, $f=1\text{MHz}$	39	pF

(1)Power dissipation capacitance per transceiver.

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At $T_A=+25^{\circ}\text{C}$, $V_{CC}=5.5\text{V}$, unless otherwise noted.

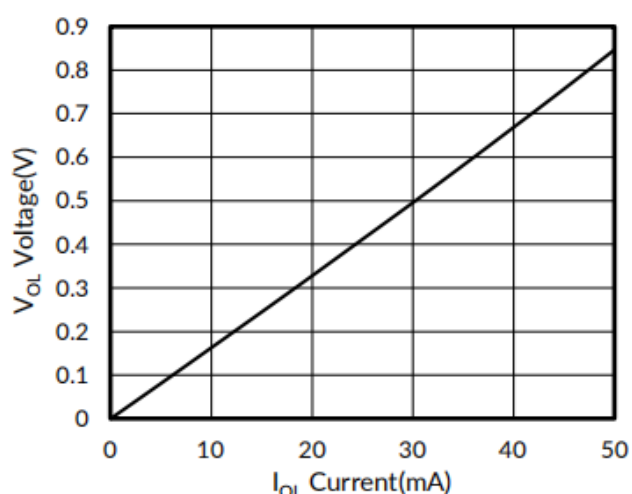


Figure 1. Voltage vs Current

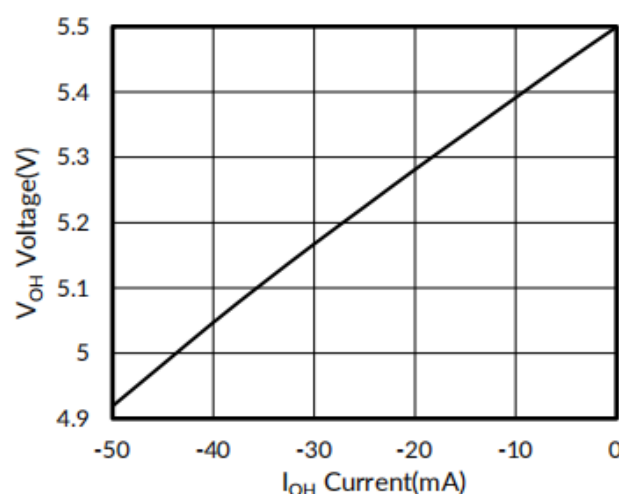
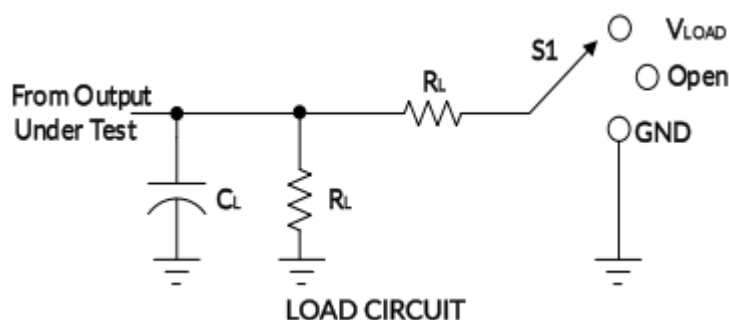


Figure 2. Voltage vs Current

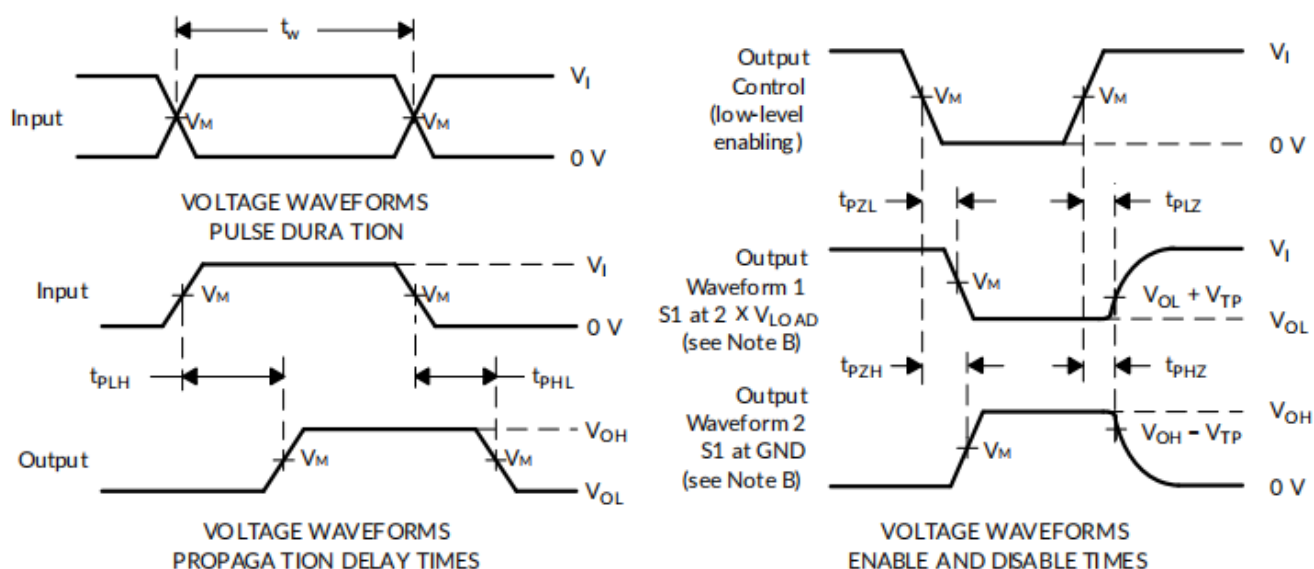


Parameter Measurement Information



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V _{LOAD}
t_{PHZ}/t_{PZH}	GND

V _{CC}	V _I	V _M	C _L	R _L	V _{TP}
5V ± 0.5V	2.7V	1.5V	15pF	2k	0.3V



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_0 = 50 \Omega$, $dv/dt \geq 1V/ns$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms



Detailed Description

Overview

The AOS244T is organized as two 4-bit buffers or drivers with separate output enable (\overline{OE}) inputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on \overline{OE} causes the outputs are in the high-impedance state. While A Low on \overline{OE} , the devices passes data from input A to output Y. To ensure the high impedance state during power up or power down, \overline{OE} must be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Feature Description

The AOS244T device can drive up to 15 LSTTL loads. This device has low power consumption of $40\mu A I_{CC}$.

The AOS244T also has 3 state outputs that allow the outputs to go to high impedance, low or high.

Application and Implementation

Information in the following applications sections is not part of the AOS component specification, and AOS does not warrant its accuracy or completeness. AOS's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The AOS244T is a high-drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

Typical Application

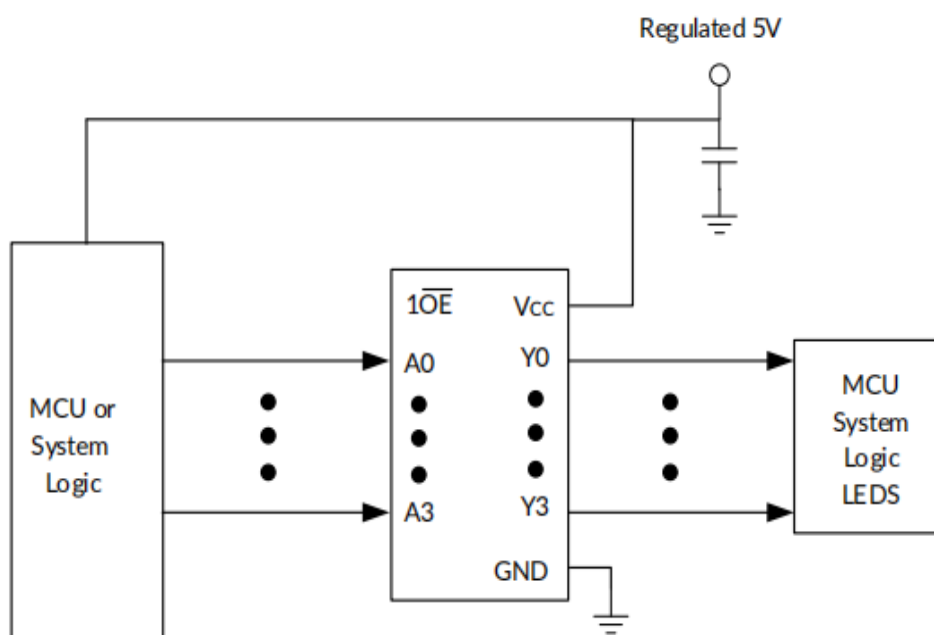


Figure 4. Application Schematic



Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents in excess of maximum limits. The high drive creates fast edges into light loads, so consider routing and load conditions to prevent ringing.

Power Supply Recommendations

The power supply pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μ F capacitor is recommended and if there are multiple V_{CC} terminals then 0.01 μ F or 0.022 μ F capacitors are recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor must be installed as close to the power terminal as possible for the best results.

Layout

Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally, they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

Layout Example

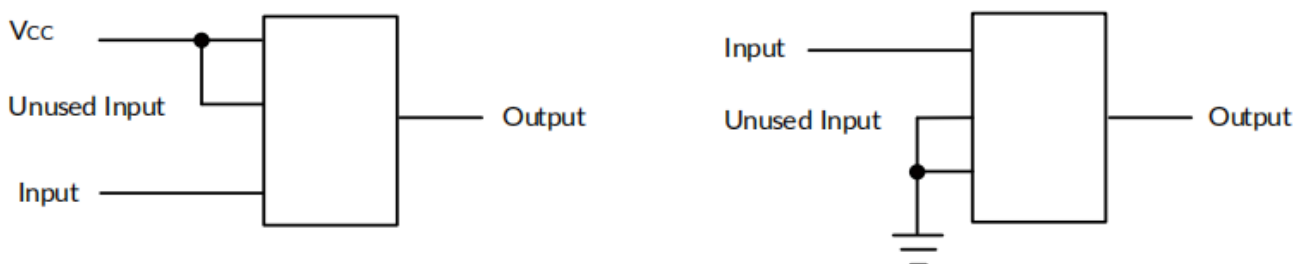
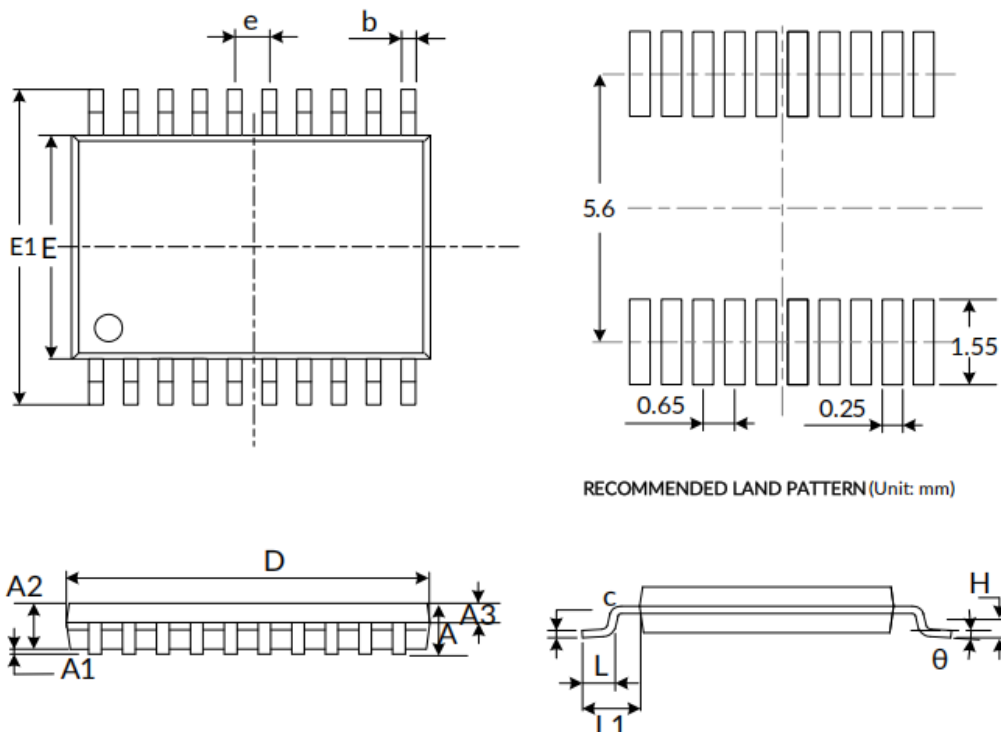


Figure 5. Layout Diagram



PACKAGE OUTLINE DIMENSIONS
TSSOP20⁽⁴⁾



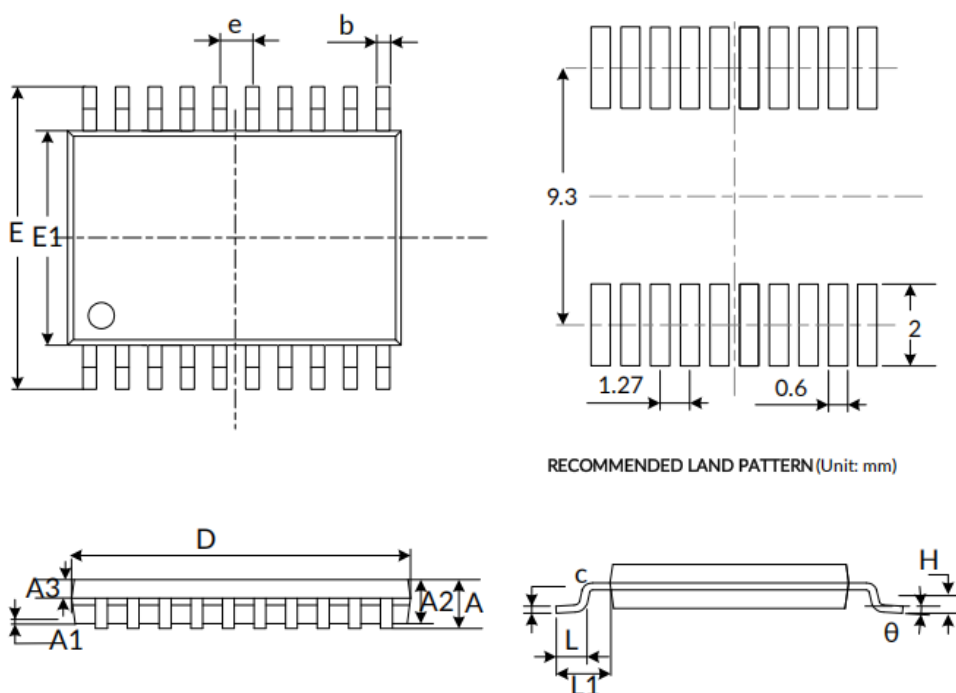
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A ⁽¹⁾		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
A3	0.390	0.490	0.015	0.020
b	0.200	0.290	0.008	0.011
c	0.130	0.170	0.005	0.007
D ⁽¹⁾	6.400	6.600	0.252	0.260
E ⁽¹⁾	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.224	0.260
e	0.650(BSC) ⁽²⁾		0.026(BSC) ⁽²⁾	
L	0.450	0.750	0.018	0.030
H	0.250(TYP)		0.010(TYP)	
	0°	8°	0°	8°
L1	1.00(REF) ⁽³⁾		0.039(REF) ⁽³⁾	

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. REF is the abbreviation for Reference.
4. This drawing is subject to change without notice.



SOP20⁽⁴⁾



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A ⁽¹⁾		2.650		0.104
A1	0.100	0.300	0.004	0.012
A2	2.250	2.350	0.089	0.093
A3	0.970	1.070	0.038	0.042
b	0.390	0.470	0.015	0.019
c	0.250	0.290	0.010	0.011
D ⁽¹⁾	12.700	12.900	0.500	0.508
E	10.100	10.500	0.398	0.413
E1 ⁽¹⁾	7.400	7.600	0.291	0.299
e	1.270(BSC) ⁽²⁾		0.050(BSC) ⁽²⁾	
L	0.700	1.000	0.028	0.039
H	0.250(TYP)		0.010(TYP)	
	0°	8°	0°	8°
L1	1.400(REF) ⁽³⁾		0.055(REF) ⁽³⁾	

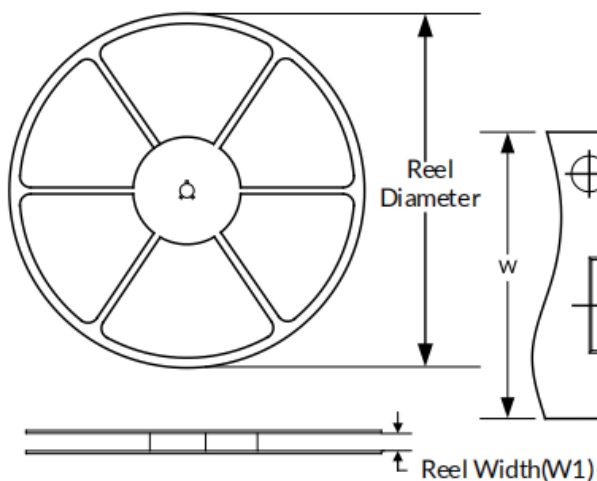
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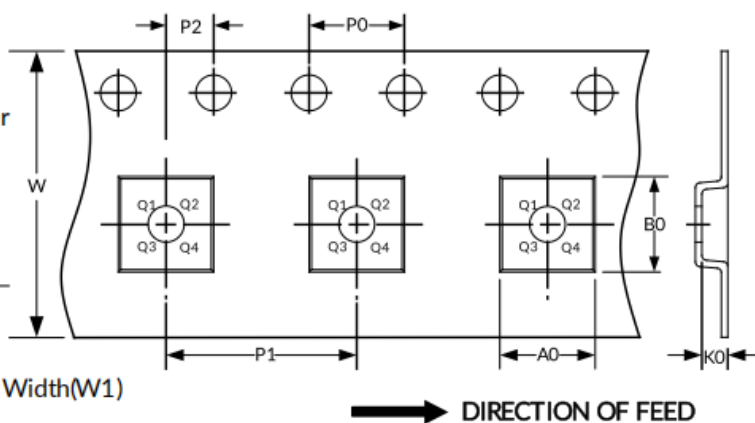


TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP20	13''	12.4	6.75	6.95	1.20	4.0	8.0	2.0	16.0	Q1
SOP20	13''	24.4	10.75	13.55	2.65	4.0	12.0	2.0	24.0	Q1

NOTE:

1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.